5 - 25 Application of the DRS Chip for Fast Waveform Digitizing

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The maximum information of a pulse from a detector can be acquired by digitizing a fast signal directly. An alternative to flash ADCs is the usage of SCA (switched-capacitor arrays)[1–2]. The input signal is sampled and stored in a series of capacitors at high sample rates under the control of a shift register, and digitized with a commercial ADC operating at lower sample rate. The DRS (Domino Ring Sample) chip developed by the Paul Scherrer Institute, Switzerland, has been designed for maximum flexibility. We choose DRS4 chip to design a waveform sampling digitizing board. Each DRS4 chip contains 9 channels, and there are 1 024 sampling capacitors in each channel. The Domino wave is generated by a series of inverters, whose speed is controlled by an analogue voltage. The DRS4 waveform digitizing board records the input signal with a high sample rate between 0.7 and 5 GS/s. The Domino wave can be stopped by an external trigger, after which the sampling capacitors are read out and digitized by a commercial ADC[3].

The overview of the waveform sampling digitizing board is shown in Fig. 1. The circuit mainly consists of a DRS4 chip, an ADC chip, a DAC chip, a FPGA and other devices. The digitizing board has eight analog channels. The DRS4 chip is capable of sampling differential input channels, so the single-end inputs need to be converted into differential signals. The on-board 16-bit DAC generates reference voltages to measure the offsets of all sampling cells for calibration, and generates offset voltages for DRS4 and buffers. The input signal has a 1 V maximum amplitude, and AC coupled mode is adopted at inputs. The data in DRS4 is read by a FPGA and a 14-bit commercial ADC. The control of the digitizing board, receiving outputs of ADC and communicating with a PC, are implemented entirely by a FPGA. The data and commands are transmitted between a PC and digitizing board via USB. The data transfer rates of the USB bus is over 20 MB/s. A comparator is used in each analog input channel for generating a triggering signal. These trigger signals from all comparators can be combined into “AND” or “OR” logic in the FPGA. Once the trigger is effective, the sampling in the DRS chip is stopped and the information stored in the SCA is digitized with an external ADC.

The digitizing board has been tested. Its bandwidth (-3 dB) is about 700 MHz, the input dynamic range is one volt. The SNR is about 66 dB, and the time resolution is approximately 50 ps. The features of the system are high resolution, low cost, low power dissipation, high channel density and small size. A typical detector signals are shown in Fig. 2. Results on energy and timing information are shown as an example, including two time signals and four energy signals. The waveform sampling readout digitizing board can be used not only for physics experiments, but also for many other different applications.

References