6 - 6 Progress and Achievements of Nuclear Electronics Group in 2022

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The main progress and achievements obtained in 2022 relays on research of nuclear electronic, development of instruments for the particle physics and nuclear experiments as usually years. The relevant interdisciplinary are briefly introduced as below:

1. Readout electronics for TPC at CEE: as one of the core detectors of the CSR External-target Experiment (CEE), the Time Projection Chamber (TPC) with high reception is used to measure the three-dimensional tracks of light charged particles and identify the charged particles. The scale of the supporting readout electronic channels is expected to reach 15 000 channels, and the maximum event rate of the L1 trigger is up to 10 kHz. A Multi-channel readout electronics system (128 ch per board) for CEE-TPC based on SAMPA ASIC has been designed and implemented. So far, we have completed the development, testing and verification of the readout system principal prototype, which has entered the stage of engineering mass production. It is expected that the entire spectrometer will be completed and installed and put into use in 2024.

2. FEE for MWDC at CEE: Multi Wire Drift Chamber (MWDC) is a fore-angle charged particle track detector at CEE. A readout electronics for MWDC has been designed and implemented, which is based on independent development Application Specific Integrated Circuit (ASIC). The FEE is based on FEAM ASIC (the Front-End Amplifier for MWDC) which is designed and fabricated in 2020 by IMP. Performance of the prototype has been characterized in the lab and commissioned with MWDC. The test results indicate that the readout system conforms to its specifications. At present, the test of engineering production is proceeding.

3. Prototype readout electronics for HFRS beam position sensitive detector: the system includes Front-End Electronics (FEE), Sub_Data Acquisition (Sub_DAQ), and Common Data Acquisition Unit (CDAU). Based on a self-developed ASIC chip, the FEE amplifies and reshapes the detector signals. The Sub_DAQ, based on a FPGA, can perform an analogue-to-digital conversion, online data processing, and package transmission before transmitting the data to the CDAU via a high-speed optical fibre link. The CDAU gathered data, online processed the data, and then transmitted the data to the computer via the PCIe 3.0 interface. The test result shows that the integral non-linearity of the system is better than 1% in the dynamic range of charge signal between 25∼900 fC and the time resolution of electronics is better than 1 ns.

4. A new digital readout system for beam position and profile monitoring: The 128-channel weak current-to-digital readout system has been designed and implemented. According to the results of laboratory test, the system can realize the non-dead-time digital reading of input signals with 128 channels in the range of 55 to 750 nA, the relative error is less than 0.5%, and the nonlinear error is less than 0.8%.

5. In terms of ASIC, three prototype ASIC has been designed and implemented. Firstly, a new ASIC for TPC detectors called FEAT has been designed which can afford 10 pC dynamic range, with 160 and 900 ns peaking time. The FEAT can directly drive a differential ADC with 2 Vpp in a waveform sampling system. Secondly, a 10 bits, 20 MS/s, low-dissipation successive-approximation-register (SAR) analog-to-digital converter (ADC), named NESAR, has been taped out. The NESAR core consumes an area of 280 μm×260 μm with an input capacitance of 320 fF. In pre-layout simulation, the power consumption of the chip is less than 2 mW. Thirdly, a 16-channel event-driven digital-analog hybrid chip named EDIMS for front-end readout electronics of position detectors (TPC) in HFRS has been taped out. The EDIMS is mainly for high count rate (1 MHz), large dynamic range of input signals (10 fC∼1 pC). Meantime, it realizes the internal storage and synchronous reading of time information and energy information.