6 - 7 The Develop Progress of Front-end Electronics for TPC Detector Based on SAMPA Chip

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Heavy ion collision has been the almost unique method to study cold and dense nuclear matter in labs. The proposed CSR External-target Experiment (CEE) will be the first large scale experiment in nuclear physics independently developed in China covering the GeV energy region. The proposed experiment CEE includes a micro-pixel beam monitor of high position resolution and wide dynamic range, a big Time Projection Chamber (TPC) of wide acceptance, a Time-of-Flight detector (TOF) capable of high counting rate and a modern dipole with large acceptance.

As one of the core detectors of CEE spectrometer, the front-end readout electronics of large time projection chamber detector with high reception can be used to measure the three-dimensional tracks of light charged particles and identify charged particles (Fig. 1).

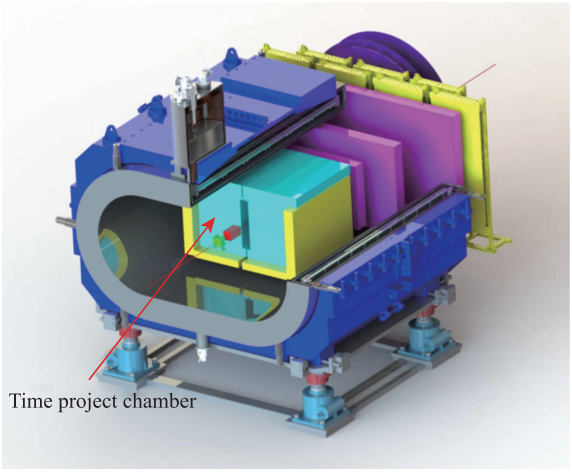

Fig. 1 (color online) General appearance of CEE spectrometer.

The scale of the supporting readout electronic channels is expected to reach 15 000 channels, and the maximum triggering event rate of the first stage will reach 1 kHz. Its successful development will play a key role in the whole spectrometer.

After pre-research and selection, we finally adopted SAMPA, an internationally advanced digital analog mixed ASIC chip, to develop the front-end readout circuit of TPC. Each circuit uses 4 SAMPA chips, which can provide 128 channels of charge-sensitive forward amplifier, amplification forming and ADC (10 bit) of 10 M sampling rate. After reading, processing and framing the detector data, the one-piece controller inputs all the high-speed scientific data into the back-end DAQ collection circuit through a fiber optic interface. According to the scale of detector, 118 FEE circuit boards are needed to complete the full read out task. Figure 2 shows the schematic diagram of a single piece of FEE hardware.

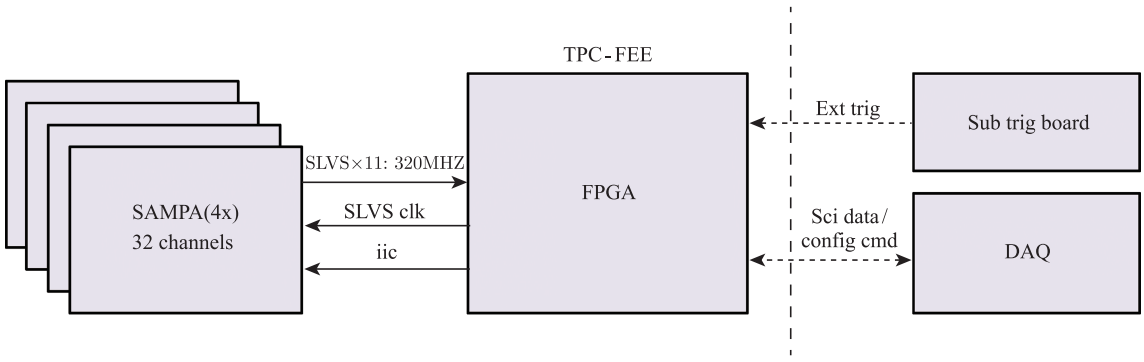

Fig. 2 (color online) The schematic diagram of a single piece of FEE hardware.

The acceptance index parameters of the readout electronic system are as follows:

(1) Total input chs: 15 000.

(2) Event rate: $\leqslant$10 KHz.

(3) INL (Lab): $\leqslant$1%.

(4) Energy resolution(Lab): $\leqslant$10%.

(5) Resolution of position: $\leqslant$500 μm.

The controller of each FEE adopts high-performance FPGA, and its control logic uses the same set of firmware. The specific functions are as follows:

(1) Initialize the FEE circuit after power-on;

(2) Receive and parse the downstream instructions forwarded from DAQ, and complete the configuration of all SAMPA chips through IIC interface;

(3) Based on the trigger working mode, under the excitation of the trigger signal, the SAMPA chip is controlled to realize the sampling, processing, digitization, framing and state parameter reading of the detector signal, and the scientific data is received by GTX IP and cached to DAQ.

(4) Control the telemetry ADC circuit of FEE, monitor key temperature and current monitoring points in TPC-FEE, read the latest monitoring data, form status data packet and return to DAQ when receiving the query instruction issued by DAQ. Figure 3 shows the structure principle of FEE FPGA firmware.

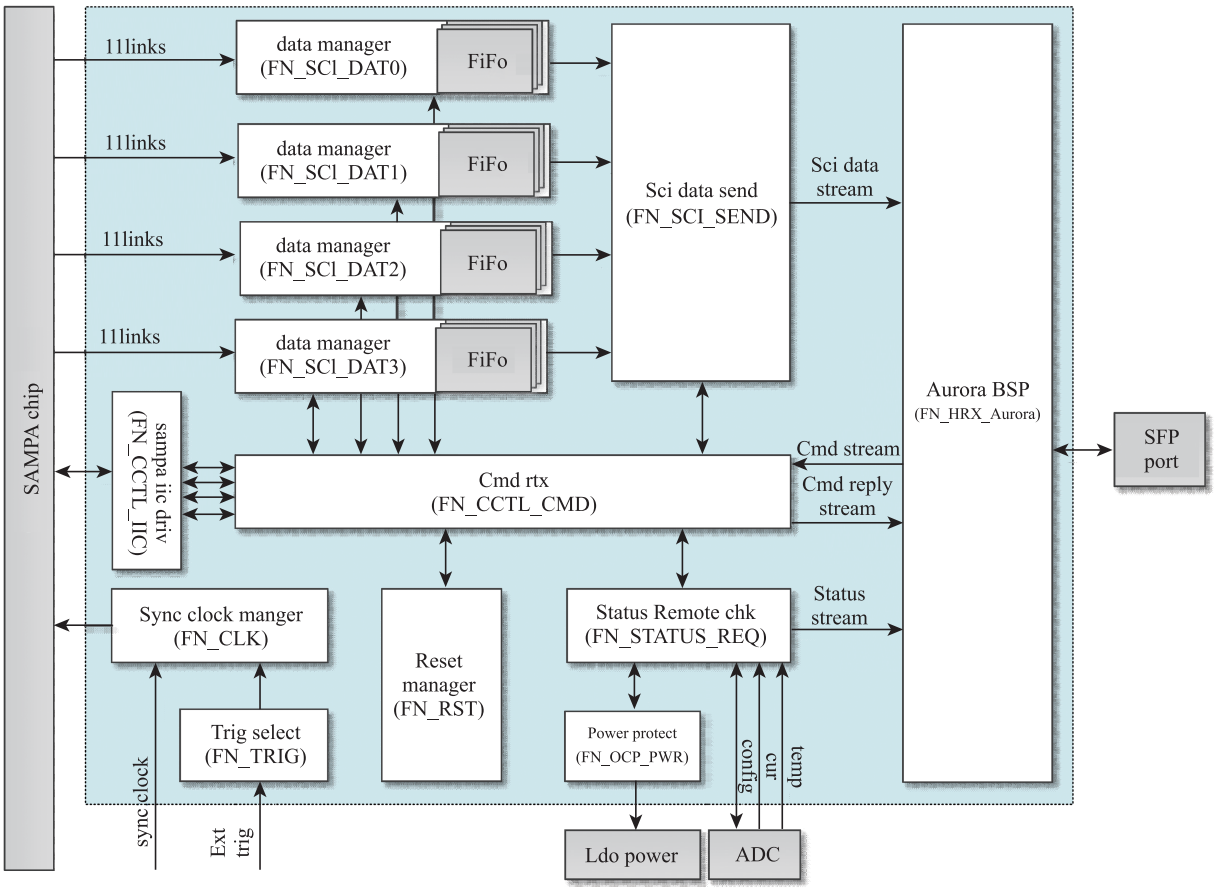

Fig. 3 (color online) The structure principle of FEE FPGA firmware.

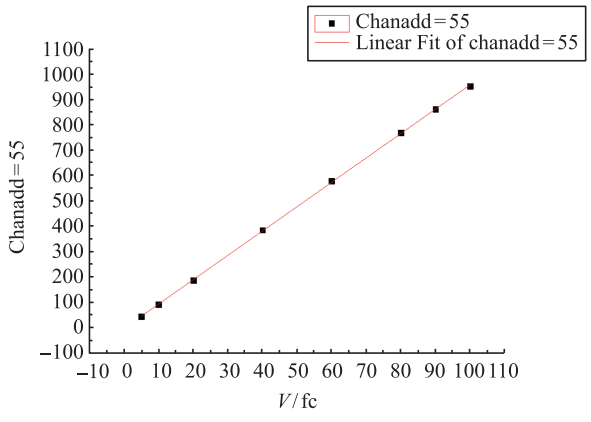

Fig. 4 (color online) Result of FEE INL test.

After the completion of the principle prototype and a large number of tests, the following key test results can be obtained:

1) INL test:

In the sampa dynamic range (1∼100 fc), the INL is less than 0.29%. The result is shown in Fig. 4.

2) Laboratory Energy Resolution test

The energy resolution of FEE is better than 10%(FWHM) when the MIP charge is 1.4 fC and the result is shown in Fig. 5.

3) Detector(384-channel principle prototype) & FEE joint test with ^{55}Fe:

The energy resolution is 26.13%, and the test result is shown in Fig. 6.

Now, we have completed the development, testing and verification of the FEE principle prototype, which has entered the stage of engineering mass production. It is expected that the entire spectrometer will be completed and installed and put into use in 2024.

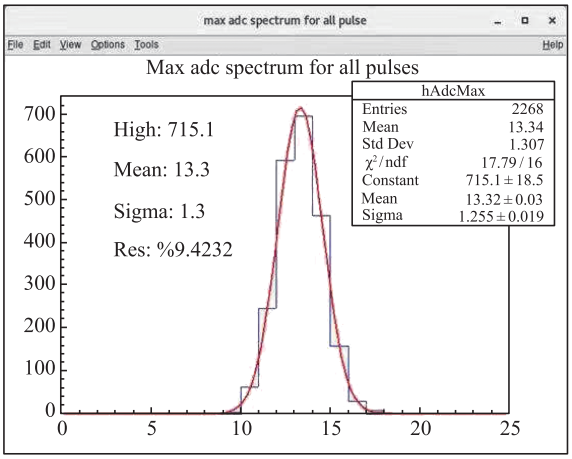

Fig. 5 (color online) Result of FEE in laboratory energy resolution test.

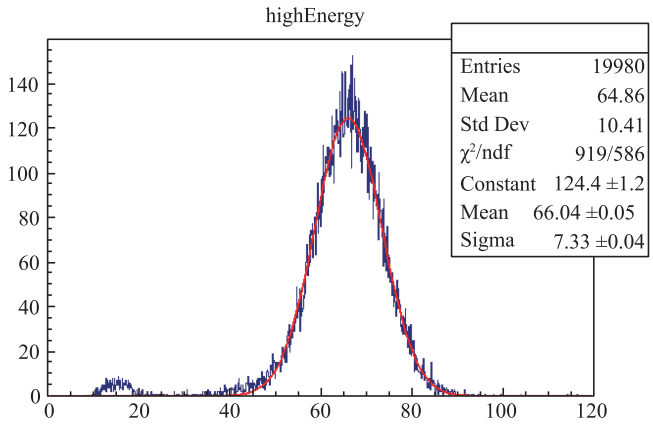

Fig. 6 (color online) Energy resolution test result of FEE joint with detector principle prototype.

6 - 8 Design of a New Digital Readout System for Beam Position and Profile Monitoring

She Qianshun

The beam position and profile uniformity monitoring detector usually output multi-channel weak current pulse signal in the beam monitoring system of the experimental terminal, but the intermittent readout system cannot accurately obtain the beam position and profile information. In order to reduce the dead time of the readout system, a new multi-channel weak current-to-digital conversion special integrated chip has been used to design the front-end readout circuit. This device has the ability of continuous signal processing, which can realize the dead-free reading of beam position and profile information. In view of the problems of low integration, large power consumption, serious heating and high cost of the existing readout system, high-integration devices are used for front-end processing, and combined with the Gigabit Ethernet transmission module on the board and the upper computer side, the main function of the beam position and profile uniformity monitoring readout system can be realized, thus greatly reducing the power consumption and area of the circuits and reducing costs. The development of a new readout system for on-line monitoring of beam position and profile can greatly improve the correctness, completeness and stability of beam position and profile uniformity monitoring at the experimental terminal, and lay a foundation for improving the utilization efficiency of beam.

The overall design of the 128-channel weak current-to-digital readout system is shown in Fig. 1. The 128-channel weak current pulse signals output by the detector directly enters the 128-channel current-to-digital conversion ASIC device ADAS1134. The device directly converts the weak current signal into a digital signal, and then transmits the data to FPGA through the serial peripheral interface (SPI). FPGA uploads the data to the upper computer for display and storage over the Gigabit Ethernet interface.

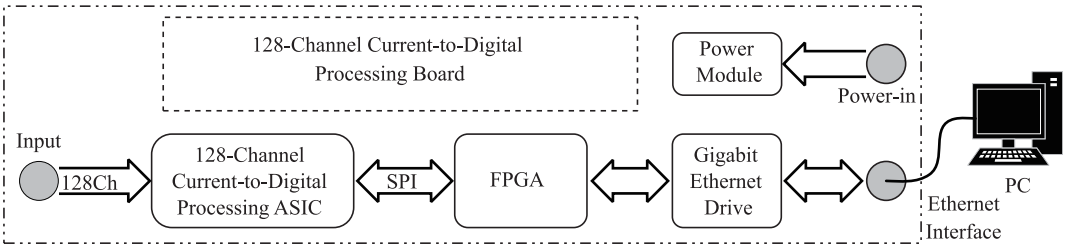

Fig. 1 (color online) The design block diagram of 128-channel weak current-to-digital readout system.