Now, we have completed the development, testing and verification of the FEE principle prototype, which has entered the stage of engineering mass production. It is expected that the entire spectrometer will be completed and installed and put into use in 2024.

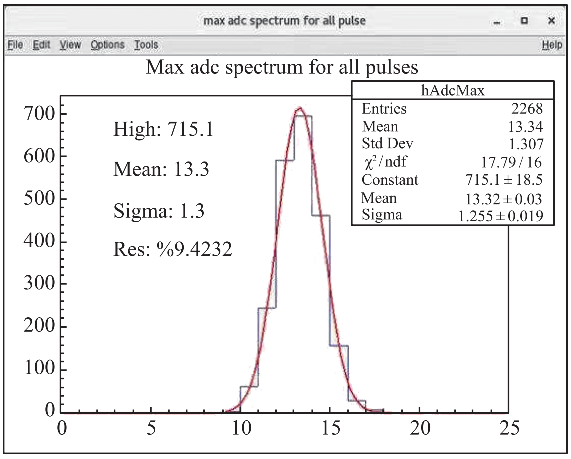

Fig. 5 (color online) Result of FEE in laboratory energy resolution test.

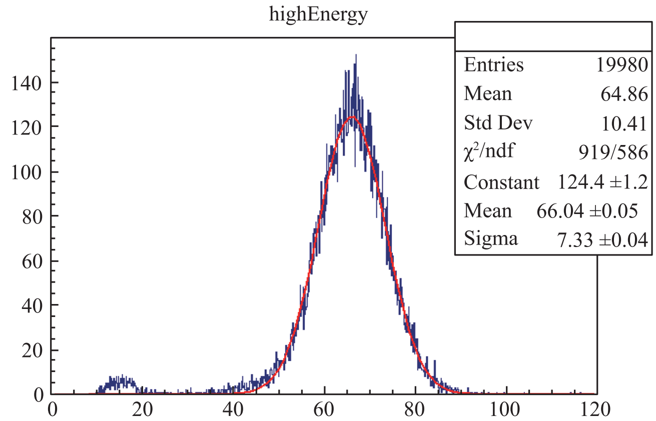

Fig. 6 (color online) Energy resolution test result of FEE joint with detector principle prototype.

6 - 8 Design of a New Digital Readout System for Beam Position and Profile Monitoring

She Qianshun

The beam position and profile uniformity monitoring detector usually output multi-channel weak current pulse signal in the beam monitoring system of the experimental terminal, but the intermittent readout system cannot accurately obtain the beam position and profile information. In order to reduce the dead time of the readout system, a new multi-channel weak current-to-digital conversion special integrated chip has been used to design the front-end readout circuit. This device has the ability of continuous signal processing, which can realize the dead-free reading of beam position and profile information. In view of the problems of low integration, large power consumption, serious heating and high cost of the existing readout system, high-integration devices are used for front-end processing, and combined with the Gigabit Ethernet transmission module on the board and the upper computer side, the main function of the beam position and profile uniformity monitoring readout system can be realized, thus greatly reducing the power consumption and area of the circuits and reducing costs. The development of a new readout system for on-line monitoring of beam position and profile can greatly improve the correctness, completeness and stability of beam position and profile uniformity monitoring at the experimental terminal, and lay a foundation for improving the utilization efficiency of beam.

The overall design of the 128-channel weak current-to-digital readout system is shown in Fig. 1. The 128-channel weak current pulse signals output by the detector directly enters the 128-channel current-to-digital conversion ASIC device ADAS1134. The device directly converts the weak current signal into a digital signal, and then transmits the data to FPGA through the serial peripheral interface (SPI). FPGA uploads the data to the upper computer for display and storage over the Gigabit Ethernet interface.

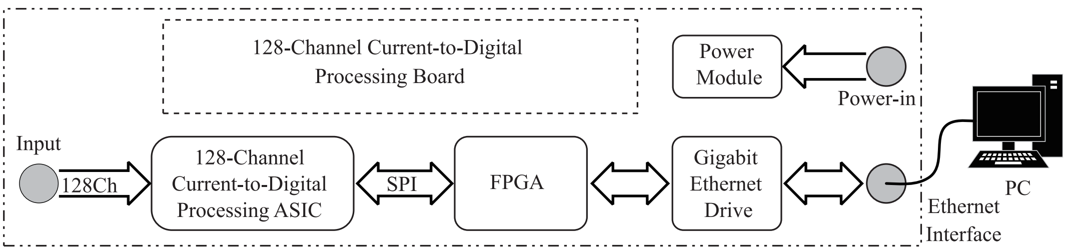

Fig. 1 (color online) The design block diagram of 128-channel weak current-to-digital readout system.

The system mainly consists of four circuit modules: 128-channel current digital conversion circuit, Gigabit Ethernet transmission module, power module, and FPGA module circuit. Among them, the 128-channel current-to-digital conversion circuit is implemented by device ADAS1134. The Gigabit Ethernet transmission module is mainly used for data transmission and parameter configuration. It is designed with a highly integrated network transmission PHY chip RTL8211EG launched by Realtek. Through the firmware design of FPGA to realize the configuration and data interaction and transmission of ADAS1134, the designed display interface of the upper computer is shown in Fig. 2.

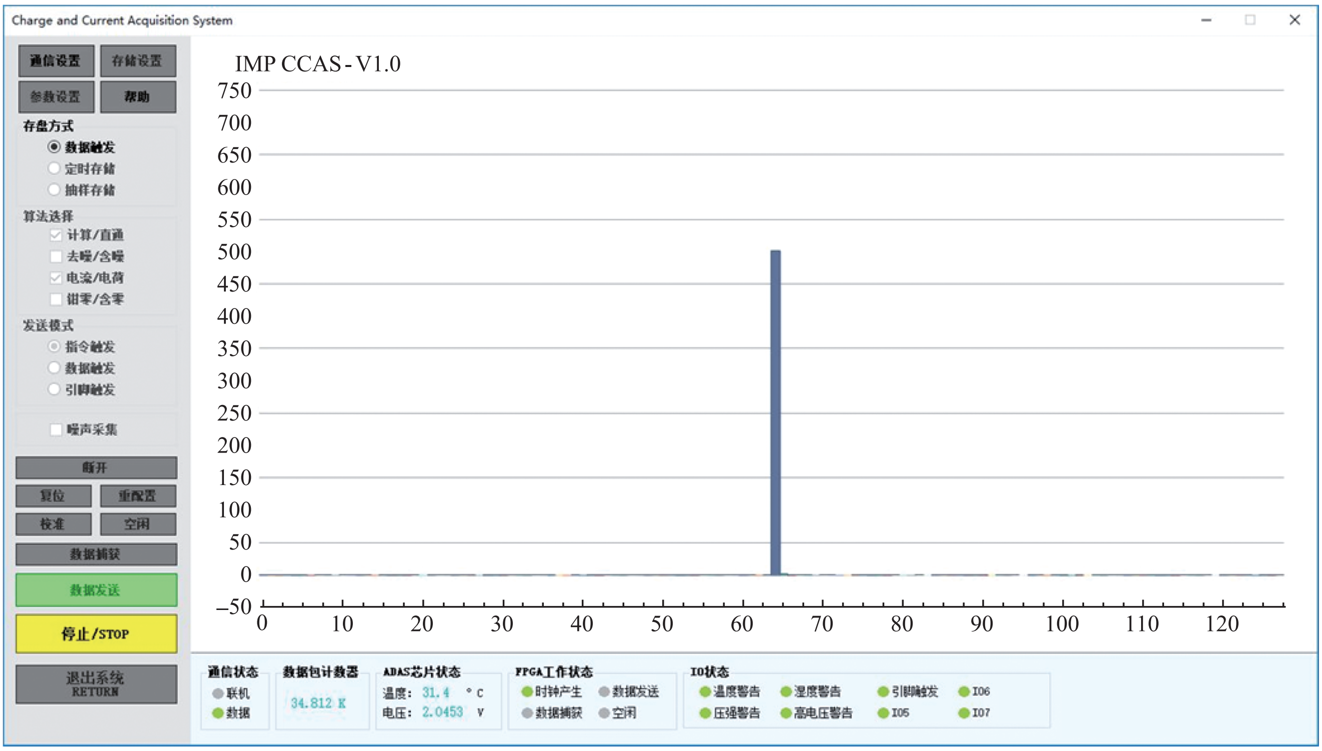

Fig. 2 (color online) The designed display interface of the upper computer.

After the laboratory testing, the system can realize the non-dead-time digital reading of input signals with 128 channels in the range of 55 to 750 nA. The relative error is less than 0.5%, and the nonlinear error is less than 0.8%. This readout system can fully meet the needs of the experimental terminal for beam position and profile monitoring.

6 - 9 Development of a Multi-channel Readout System Based on Self-developed ASIC Chip for CEE-MWDC

Yan Junwei, Pu Tianlei, Qi Yi, Kong Jie, Xu Jiapeng, Yang Zuoqiao and Li Feng

The CSR External-target Experiment facility (CEE) will be the first large scale experiment in nuclear physics independently developed in China covering the GeV energy range. The Multi-Wire Drift Chamber (MWDC) is among the significant detectors for CSR-CEE, with more than 3 200 analog input channels. Considering the needs of readout on such a large scale, it is urgent to develop a readout system which are suitable for high integration, high count rate and large dynamic range in order to measure the tracks of fore-angle products. To achieve the event rate up to 10 kHz and 1 pC dynamic range, the readout system is based on one self-developed ASIC chip named FEAM, the Front-End Amplifier for MWDC, as well as the SCA chip for digitizing is equipped on DAQ board. As depicted in the following figure, the 96-channel prototype of readout system developed by our group is consists of three front-end electronics (FEE) boards, a data acquisition (DAQ) board as well as a Host PC (Fig. 1). The FEE circuit is a key module in the newly developed readout system, it will be described in detail bellow.