5 - 20 The Effects of Total Ionizing Dose on the SEU Cross-section of SOI SRAMs*

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The single event effect (SEE), total ionizing dose (TID) effect, and synergy between the TID and SEE in electronic devices have been extensively studied. Schwank, *et al.*, have irradiated many kinds of static random access memory (SRAM) devices with various radiation sources, such as γ-ray, X-ray, and proton, and then measured the single event upset (SEU) cross-section of the devices. The experimental results showed that the TID irradiation has a significant effect on the SEU cross-section of the device, and the SEU cross-section increases with increasing irradiation dose. Meanwhile, the SEU cross-section had a certain dependence on parameters such as test data patterns, irradiation test temperature, *etc.*[1−4].

We design two silicon on insulator SRAMs with different layout structures, based on the 130 nm SOI CMOS process. Figure 1(a) shows a schematic diagram of the layout structure and size of the 6T SRAM cell with dimensions 3.7×3.2 μm. The access transistors N3 and N4 share drain electrodes with the pull-down transistors N1 and N2, respectively. Figure 1(b) shows the layout structure and size of the 7T SRAM memory cell after hardened design by the delay transistor N5. The cell size of the 7T SRAM is 3.9 μm×3.4 μm. The gate electrode of the delay transistor N5 is connected to the gate electrode of the access transistors N3 and N4. During the read/write operation, the delay transistor N5 will be in the ON-state, which has a very low resistance. While the delay transistor N5 will be in the OFF-state when the data hold state is entered, and the resistance of OFF-state N5 is very high, which can effectively suppress the single-event transient disturbance and significantly improve the stability of the 7T memory cell.

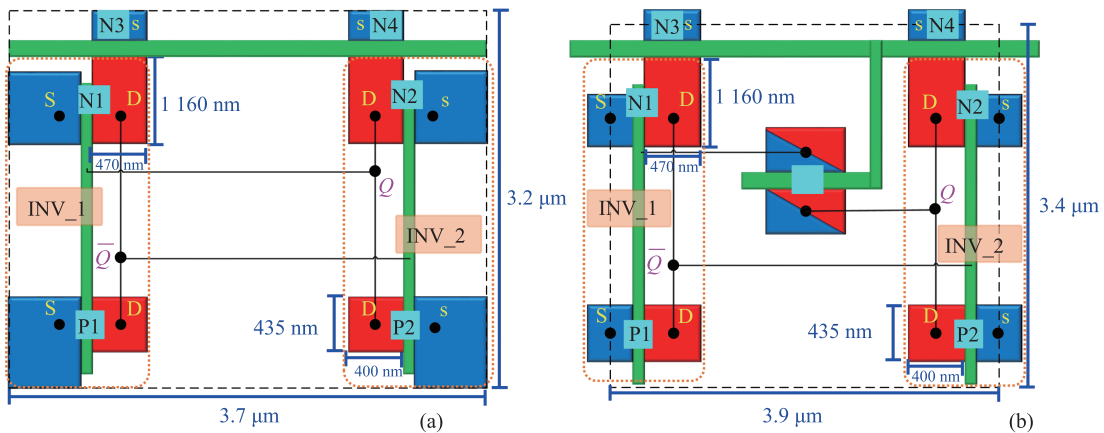

Fig. 1 (color online) Schematics of memory cell structure of (a) 6T SRAM, (b) 7T SRAM.

Figure 2 shows the SEU cross sections of 6T SRAM and 7T SRAM characterized by Bi ions (99.8 MeV · cm^2/mg) as a function of TID. The SEU cross sections of 6T SOI SRAM characterized by Bi ion are also increased by TID. As shown in Fig. 2(a) and (b), SEU cross section of 6T SRAM increases by a factor 9.1%(55h) and 4.0% (AAh) of after deposition 800 krad(Si) with respect to the fresh condition. Similarly, we did not observe a significant correlation between the SEU cross section and the data pattern applied during TID exposure for 7T SRAM. Interesting to note, however, is that the SEU cross section of the 7T SRAM shows an opposite changing trend to the 6T SRAM. As shown in Fig. 2(a) and 2(b), SEU cross section of 7T SRAM decreases by a factor 42.9% (55h) and 56.6% (AAh) of after deposition 800 krad(Si) with respect to the fresh condition. Because the 6T SRAM and 7T SRAM were fabricated in the same wafer, the physical dimensions, and electrical characteristics of all transistors (N1, N2, N3, N4, P1, P2) in the memory cell are identical except for the delay-hardened transistor N5. Hence, we can conclude that the change in the electrical characteristics of the N5 is responsible for the reduction in the SEU cross section of the 7T SRAM after TID irradiation. Furthermore, we investigated the TID effect on the $1\rightarrow0$ upset and $0\rightarrow1$

upset for 7T SRAM SEU types. As shown in As shown in Fig. 2(c) and (d), the mean $1 \rightarrow 0$ upset cross section of 7T SRAM decreases by a factor 3.1% (55h), 37.9% (AAh) of after deposition 800 krad(Si) with respect to the fresh condition, and the mean $0 \rightarrow 1$ upset cross section decreases by a factor 37.9% (55h), 66.7% (AAh) of after deposition 800 krad(Si). Therefore, the decrease of $0 \rightarrow 1$ upset cross section is mainly responsible for the decrease of 7T SRAM SEU cross section.

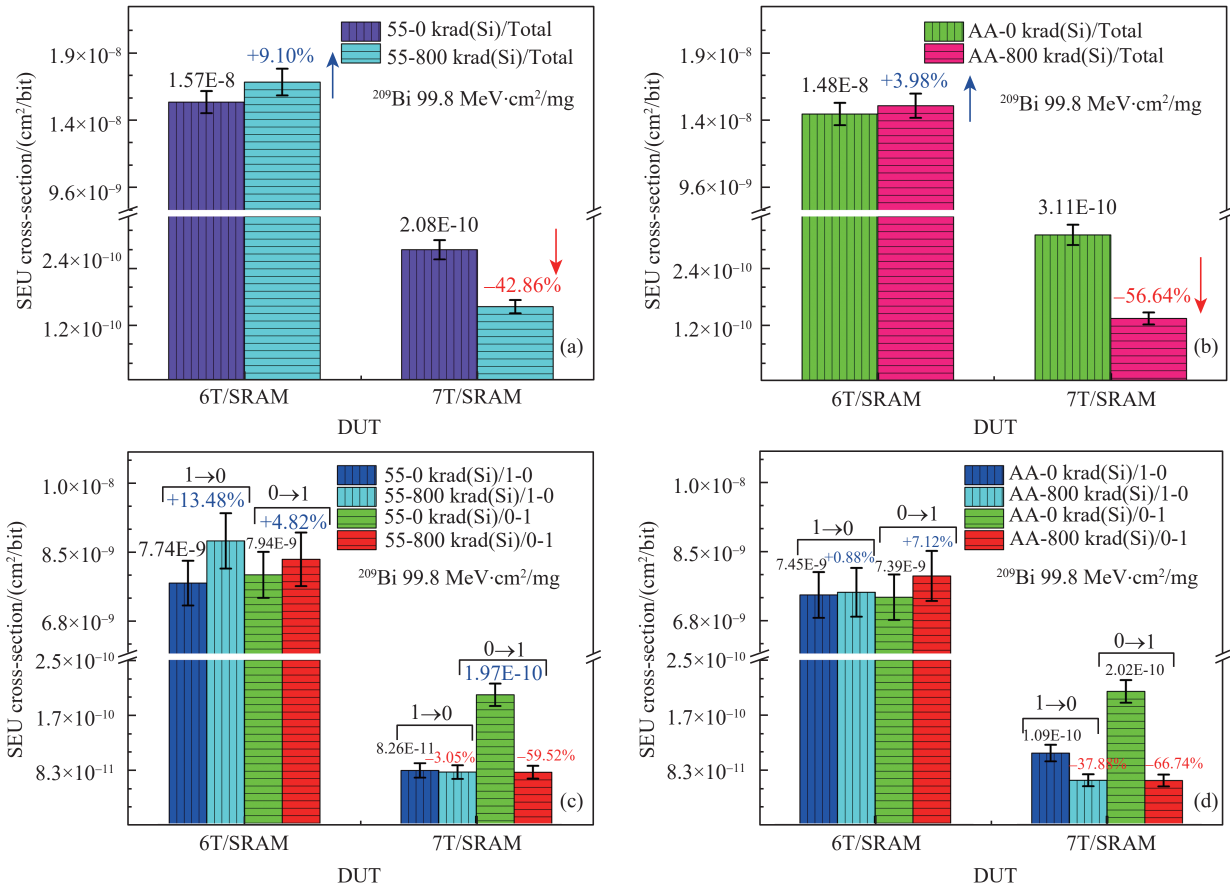

Fig. 2 (color online) SEU cross sections characterized by Bi ion versus layout structure for 6T and 7T SOI SRAMs after deposition 800 krad(Si).

The TID effects on SEU hardness of SOI SRAMs with 6T and 7T cell designs were explored in this paper. Experimental results show that the SEU cross-section of 6T SOI SRAM is increased by TID and has no dependence on the data pattern applied during TID exposure. However, it is interesting to note that the SEU cross-section of 7T SRAM decreases significantly after TID exposure. Furthermore, in our experiment, opposite changes intendencies of SEU cross-section for 6T and 7T SOI SRAMs were observed after TID irradiation. The mechanism behind the experimental results of 6T SRAM is that OFF-state leakage of pull-down nMOSEFTs increases after TID irradiation, since the parasitic transistor is turned ON by radiation in the shallow trench isolation oxide (STI) region. However, the radiation-induced decrease in carrier mobility in delay transistor N5 of the 7T SRAM is responsible for the decrease of the SEU cross-section. Because radiation-induced charges trapped in the STI and buried oxide (BOX) improve the carrier scattering rate, the OFF-state equivalent resistance of delay transistor N5 increases, causing the stronger suppression of transient pulses and feedback signals, ultimately leading to SEU cross-section decreases. Our experimental results provide a new insight into the radiation-hardened by design (RHBD) used in nano-ICs.

References

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5 - 21 Differences in MBUs Induced by High-energy and Medium-energy Heavy Ions in 28 nm FPGAs*

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The high performance and flexible configuration ability of static random-access memory (SRAM)-based field-programmable gate arrays (FPGAs) make them widely used in space missions[1]. However, they are sensitive to single event upsets (SEUs) caused by heavy ion incidence[2]. Moreover, as the feature size continues to shrink, the reduction of critical charges and the enhanced ment of charge sharing effects in FPGA lead to multiple-bit upsets (MBUs) occurring more frequently[3]. MBU occurs when a single particle deposits energy into several memory cells of the same words to simultaneously upset them. When MBUs occur in critical configuration RAMs (CRAMs) that are used to configure critical system functions, on-orbit FPGA systems will face serious failures[4]. Therefore, it is mandatory to conduct an MBU evaluation of CRAMs on advanced FPGAs before their application in aerospace.

In this study, we conducted high-energy and medium-energy heavy ion tests on 28 nm FPGAs. The effects of heavy ions with different energies on the MBUs were thoroughly investigated. High-energy ^{78}Kr and medium-energy ^{129}Xe heavy ion experiments were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) in the Institute of Modern Physics, Chinese Academy of Sciences. The irradiation experiments of ^{78}Kr ions with an initial energy of 60 MeV/u and ^{129}Xe ions with a initial energy of 19.5 MeV/u were compileted at the high-energy radiation effect terminal and terminal No.5, respectively.

The detailed MBUs induced by ^{78}Kr ions were extracted, as shown in Fig. 1(a). It can be seen that compared with the 1.0 V, the 0.9 V radiations induced a higher proportion of and larger scale MBUs. Additionally, we found that compared with 13.3 and 31.0 MeV·cm^2/mg, ^{78}Kr ions with an linear energy transfer (LET) of 20.8 MeV·cm^2/mg can cause higher percentages of greater-than-3-bit MBUs in vertical radiations at 0.9 and 1.0 V, and greater-than-4-bit MBUs in tilted radiations at the 0.9 V operation. This is related to the different influence ranges and abilities of the ionization tracks. Because the $(\theta=0°, \psi=30°)$ ion trajectories covered more cells, the largest 6-bit MBUs appeared even at the LET of 13.3 MeV·cm^2/mg, which identified the worst influences in this study.

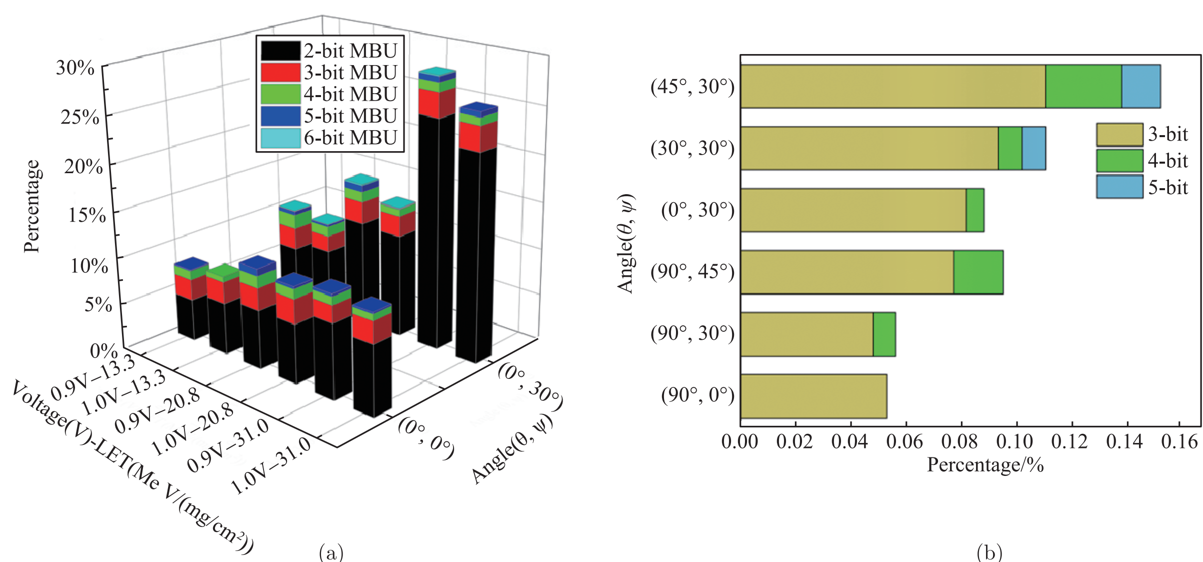

Fig. 1 (color online) Detailed percentages of different type MBUs induced by (a) ^{78}Kr and (b) ^{129}Xe ions at different conditions.

The detailed results of greater-than-2-bit MBUs induced by ^{129}Xe ions are shown in Fig. 1(b). Only the largest 3-bit MBUs were found at $(\theta=90°, \psi=0°)$. When setting $\theta=90°$ while rotating ψ, we captured MBUs no larger than