5 - 22 Heavy Ion-induced MCUs in 28 nm SRAM-based FPGAs: Upset Proportions, Classifications, and Pattern Shapes*

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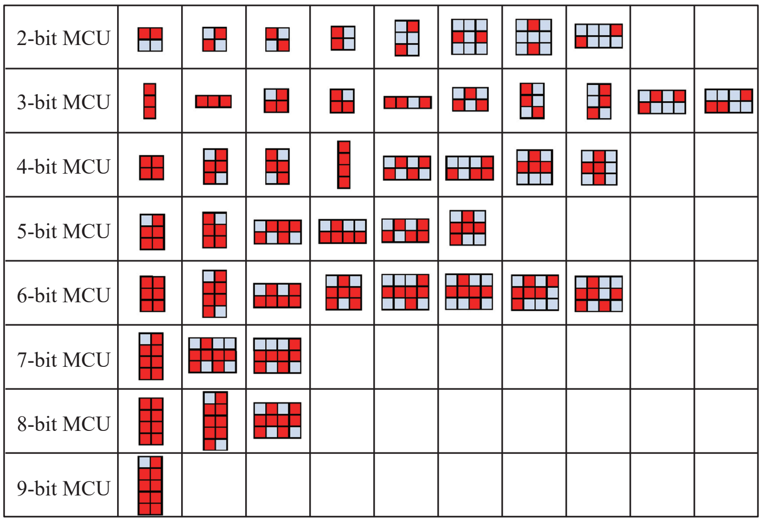
Static random-access memory (SRAM)-based field programmable gate arrays (FPGAs) are sensitive to radiation-induced single event upsets (SEUs)[1]. Single-bit upsets (SBUs), as a well-known effect in FPGAs, occur when the energy deposited by a single particle (such as heavy ion) exceeds the critical charge in single memory cell. However, in modern advanced process technologies, owing to the smaller area and decreased critical charge of transistors, a single particle can affect more than one memory cell simultaneously in the physical layout to generate clustered errors, that is, multiple cell upsets (MCUs)[2]. MCUs have become a catastrophic factor that threatens the safety of FPGAs applied in aerospace missions[3]. Particularly, as the feature size of transistors continuously shrinks to the nanoscale, the proportion of MCUs in FPGAs increases dramatically[4]. When MCUs occur in critical configuration RAMs (CRAMs) that control the entire functions of FPGAs, an abnormal state of the on-orbit systems may occur. Therefore, it is crucial to study the impact of MCU on CRAMs to guarantee the safety of critical electronic components in aerospace missions.

In this study, systematic heavy-ion irradiations on 28 nm SRAM-based FPGAs were performed to determine the worse MCU response of devices, and an improved MCU extraction method was proposed to study the MCU features. Irradiation tests were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences. High-energy ^{78}Kr ions and medium-energy ^{129}Xe ions were used to irradiate the device under test (DUT). The ^{129}Xe ions were accelerated using a sector separator cyclotron. The ^{78}Kr ions were from the cooling storage ring (CSR), and this was the first available high-energy single-event experiment of the CSR heavy-ion accelerator.

Table. 1 Logical sizes and shapes of different MCUs.



The extracted logical sizes and shapes of the MCUs are presented in Table 1. We obtained diverse (up to 9-bit) MCU patterns based on the selection of the worst irradiation parameters; these MCU data can support an effective radiation hardening process in harsh space environments. The percentages of MCUs of different sizes are presented in Fig. 1(a) (for ^{78}Kr ions) and Fig. 1(b) (for ^{129}Xe ions). It is clear that for the high linear energy transfer (LET) ^{129}Xe ions, approximately 60% MCUs were the major problem for aerospace electronic systems. In Fig. 1(a) and (b), an apparent percentage dependence of the large (more than 3-bit) MCUs on the LET and tilts was observed, and the good consistency indicated that the MCU distinction method is suitable for high-density FPGAs. Under the same LET, all large MCUs were generated under tilted incidence, which also proved the effectiveness of the MCU extraction method.

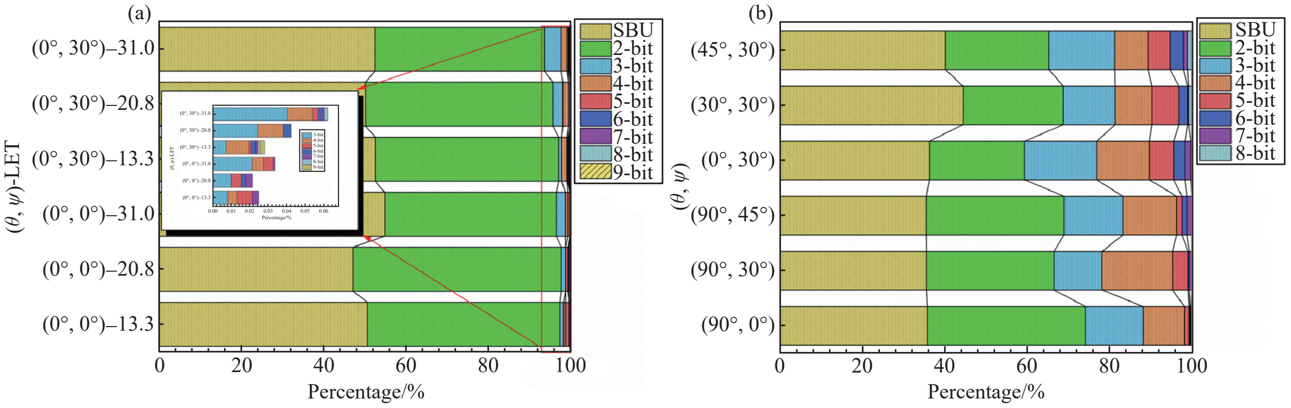


Fig. 1 (color online) Percentages and sizes of MCUs induced by (a) ^{78}Kr ions and (b) ^{129}Xe ions.

Although the SBUs and 2-bit MCUs occupied almost the entire ^{78}Kr upset dataset, when the LET was 13.3 MeV·cm^2/mg and the tilt was $(\theta = 0°, \psi = 30°)$, 9-bit MCUs were observed twice in an individual irradiation round. Compared with the maximum 8-bit MCUs found in the ^{129}Xe tests with the same $(\theta = 0°, \psi = 30°)$ incidence, the ^{78}Kr ion-induced larger MCUs revealed that although the high-energy heavy ions have a much smaller LET, the generated charges can still exceed the critical charge of the 28 nm FPGAs. Therefore, the ^{78}Kr ions have more severe effects than the ^{129}Xe ions, even with a considerably higher LET.

With detailed analysis of MCU information, we identified the worse impacts of high-energy heavy ions than medium-energy ones and different MCU features under various irradiation conditions. Worse radiation evaluations and detailed MCU extractions are indispensable for pre-applied digital circuits in harsh space environments. The worse MCU data and detailed analysis presented in this paper can be used to perform targeted hardened strategies to mitigate destructive MCUs and further control soft error rates.

References

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