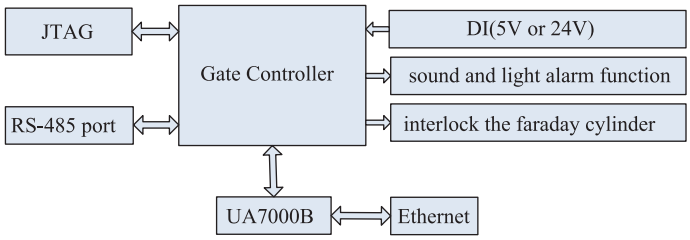

Fig. 3 (color online) Structure of the Gate Controller.

(4) To monitor the logic status of equipments remotely, DI was designed to detect the status of 5 V or 24 V inputs;

(5) The controller is configured with a unique IP address, and the upper layer connects and accesses the controller via IP and port numbers;

(6) RS485 ports were specially designed for serial devices. By appropriate algorithm and the serial interfaces, the controller and equipments could realize the data communication with each other. Meanwhile, all kinds of controllers could cascade with each other used RS485 communication interface.

The controller which has been debugged completely in 2016 is used successfully to complete status monitoring about 10 doors in the regines of ECR and CSRe.

Hardware configuration and software development for the Gate Controller are designed based on IAR and C language. With the corresponding of the software program, the Gate Controller has been working stably and met fully the requirements of the personal safety interlocking system for HIRFL-CSR.

References

[1] MSP43016xx Family User's Guide, Texas Instruments Incorporated, (2011).

[2] Detai Zhou, Yanyu Wang, IMP & HIRFL Annual Report, (2011)209.

[3] Detai Zhou, Yanyu Wang, IMP & HIRFL Annual Report, (2013)206.

6 - 35 Design of Digital and Analog Mixed Controller Based on MSP430F149

Ni fafu, Wang Yanyu and Yin Jun

In order to meet the requirements of collection the various types of electronic data which has signals with relatively slowly speed in the site of HIRFL in IMP, a new hardware controller which is combined with digital inputs outputs(DIOs) and analog inputs outputs(AIOs) was designed. Fig. 1 shows the hardware structure.

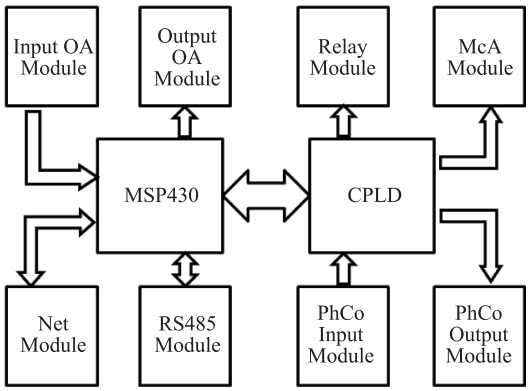

Fig. 1 The structure of controller.

As shown in Fig. 1, the board is consisted of different functional blocks. The AIOs is made up by input or output operational amplifier(OA) modules, because of the analog input or output range of MSP430F149 is from 0 V to +3.3 V[1], inserting the OA module can enlarge the scale of analog input or output up to +10 V. One kind of the DIOs is digital I/O port with Photoelectric Coupler module (PhCo input/output Module) which can get or

set 4 channels digital signal status on high or low respectively, and the corresponding electrical signal level is 0 V or +5 V. The other DIOs blocks are relay and Multichannel Alarm (McA) module. The 8 channel relay module canrealize +24 V remote contact control or seting as dry contact. The other 8 channels complete local sound-light alarming which could be set as the level or contact alarm for the specific using. The board communicates with upper computer by net module or through the port of RS485 which also could place as cascade using.

After finish of designing the controller, we measured the AIOs channels. The linear fitting curve graphic and channel conversion code frequency histogram of ADC (0∼+10 V) are shown in Fig. 2 (a) and (b), the input and output relationship graph of DAC (0∼+10 V) and specific voltage point of sampling wave are displayed in Fig. 2 (c) and (d). The ADC channels Integral Nonlinearity (INL) error could be better than 0.4% and the DAC INL is better than 0.2% [2].

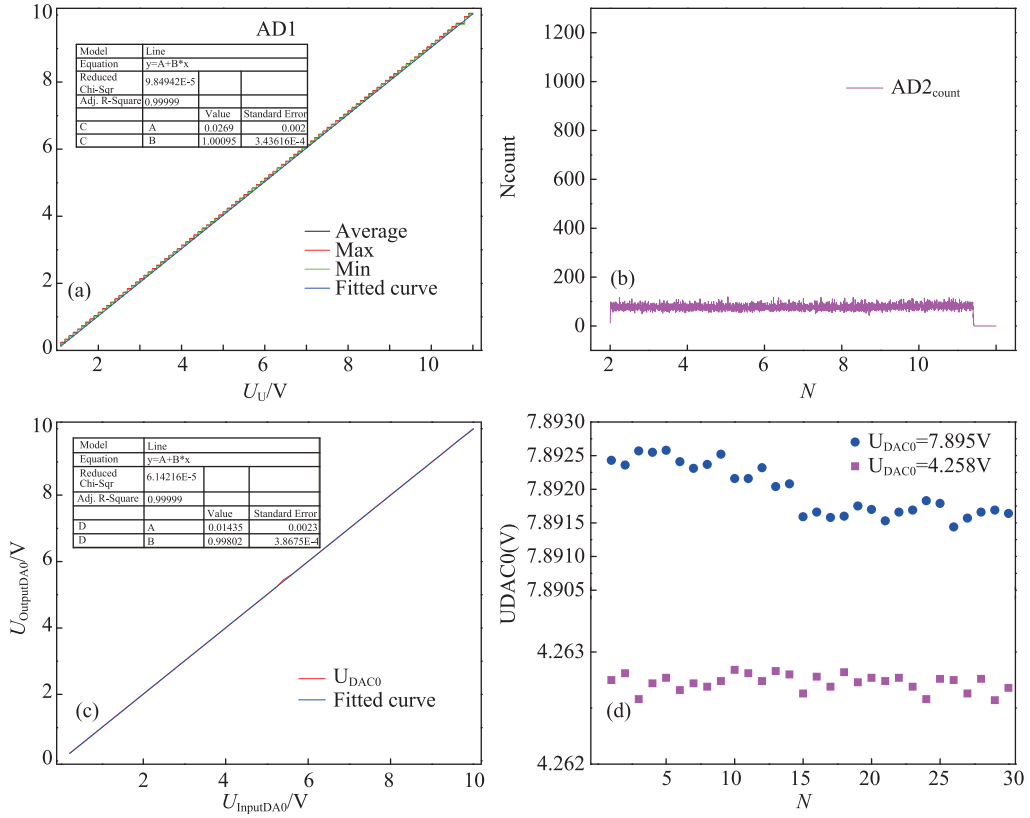

Fig. 2 (color online) Results of the AIOs.

References

[1] MSP430F16xx Family User's Guide. Texas Instruments Incorporated, (2011).

[2] Fafu Ni, Design of Accelerator Integrated Alarm Platform, 2016. (in Chinese)