6 - 35 SFC High-frequency Signal Input Circuit Fault Analysis

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The Dee voltage of the RF cavity in cyclotron HIRFL-SFC is not high enough when resonance frequency is 8.536 MHz. By repeatedly measuring and adjusting the parameters of the cavity and transmitter tank circuit, Dee voltage can only be added to 40 kV, which doesn't meet the physical requirement of 80 kV.

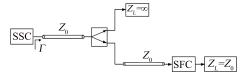
One output port of the RF divider is open circuit in the process of inspection which was discovered occasionally. SFC signal comes from the SSC, which is divided into two (see Fig. 1), but the one open suspension through 4.4 m 50 Ω coaxial cable and don't connect the load. After removing the cable from the divider, the Dee voltage of SFC could be added to 70 kV easily. At the same time the value of amplitude stability gain is lower than usual, the input signal amplitude that is too high. The value changes from 240 to 440 mV when measuring the input signal with an oscilloscope, the reason is caused by 4.4 m terminal open line. The analysis and conclusions are as follows.

1. The calculation of SSC actual input signal

When broken open line, as shown in Fig. 1, the output impedance is infinity. Because divider has isolation load, there have no effect on the SFC input signal. SFC input and SSC output are all the standard 50 Ω coaxial cable, which is exactly match without reflection.

Measurement the SFC input signal is 440 mV, so according to the 3 dB principle of the divider,

$$\overline{V}_{\rm SSC} = \sqrt{2}\overline{V}_{\rm Sfc\,1} = 440 \times \sqrt{2} \approx 622~{\rm mV}$$
 .



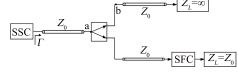


Fig. 1 Open circuit principle diagram.

Fig. 2 The principle of the open access line

2. The calculation of reflection coefficient caused by the open line

The length of the open line is L=4.4 m, the working frequency f=8.563 MHz and the working wavelength is λ =35.1453 m.

$$Z_1 = -jZ_0 \operatorname{ctg} \beta L = -jZ_0 \times 0.9976 \approx -50j$$
 , Among them, $\beta = \frac{2\pi}{\lambda}$ and $Z_0 = 50 \Omega$.

As shown in Fig. 2, assuming the impedance of point a is Z and point b is Z_1 , so the reaction impedance is Z_2 . From point b to point a. The impedance Z of point a is equal to the parallel of shunt impedance Z_2 and SFC input impedance Z_0 .

$$Z_2 = Z_0^2/Z_1 = 50j \quad Z = \frac{Z_0Z_2}{Z_0 + Z_2} = 25 + 25j \quad . \label{eq:Z2}$$

The reflection coefficient see from output of SSC is,

$$\Gamma = \left| \frac{Z - Z_0}{Z + Z_0} \right| = \frac{\sqrt{5}}{5} \approx 0.447$$
.

3. The calculation of divider input signal

$$\overline{V}_{\rm in} = \overline{V}_{\rm ssc}(1-\varGamma) = 662 \times (1-0.447) \approx 344~{\rm mV}~.$$

So the SFC signal amplitude (with 4.4 m long terminal open cable) is

$$\overline{V}_{\rm sfc2} = \overline{V}_{\rm in} \times \frac{\sqrt{2}}{2} = 344 \times \frac{\sqrt{2}}{2} \approx 243 \quad {\rm mV} \ . \label{eq:Vsfc2}$$

4. Conclusion

The theory of calculation and analysis results are consistent to the measured results with oscilloscope. The value of oscilloscope measurement 240 mV is less than the calculated value 243 mV which is caused by the loss of the divider and calculation error.

Inspired by the above analysis, there is no ideal open circuit and short circuit in high-frequency circuit. Any port and the mismatch of a transmission line have affect the RF signal transmission, but only high frequency more severely affected. Usually the low frequency characteristics of the circuit element would lose the original meaning in the high frequency circuit. Therefore, the wiring and circuit design in high frequency must be stricted and specificated.