6 - 9 LLRF Control System

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This LLRF control system operating frequency is 162.5 MHz, independently developed by IMPCAS, which consists of RF signal modulation front end, and digital signal process FPGA. The system mainly implements superconductive cavity resonance frequency control, cavity voltage amplitude stability control and phase stability control. The experimental test is completed with a model cavity developed by IMPCAS in room temperature. The twelve-hour test results show that the amplitude stability is 0.32% (peak to peak), ±0.18% (RMS), and the phase stability is ±0.35 degree(peak to peak), ±0.09 degree(RMS).

One of the superconductive cavities is half-wave length resonator, developed by IMPCAS. The load Q of this cavity is at work, The LLRF control system is designed to achieve the requirement of 0.6% for field amplitude stability, ±0.7° for phase stability, and, ±0.6° for tuner detuning phase. Since the cavity has high load Q and narrow bandwidth (about 200 Hz) features, a LLRF control system based on IQ quadrature demodulation techniques is developed and tested in room temperature. The frame diagram of LLRF is shown as Fig. 1.

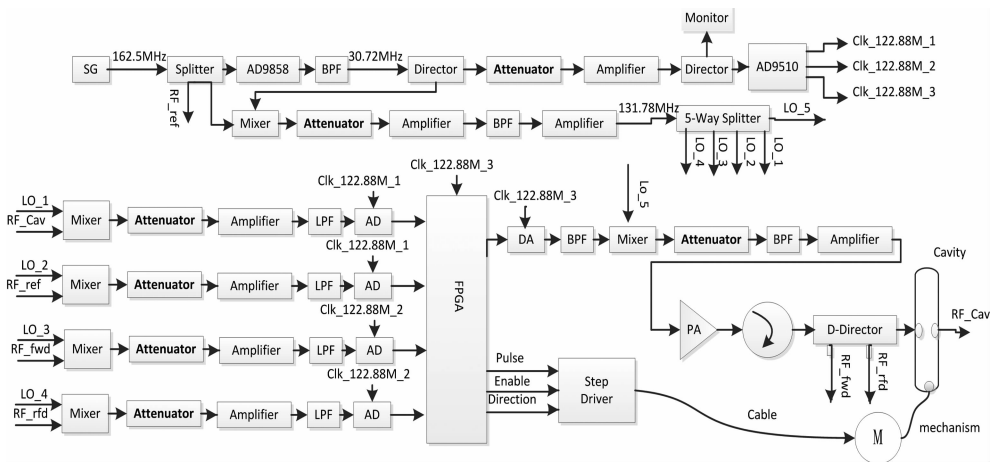

Fig. 1 The schematic of LLRF control system for 162.5 MHz radio frequency system.

In general, the hardware of LLRF system can be divided into four function blocks, which are described as the radio frequency signal modulation front end, the clock generation and distribution, digital signal processing FPGA, and 1000 M Ethernet communication. LLRF system has two layers. The bottom layer is used to put power supply module, AD9858 DDS board, AD9510 clock distribution board, ADC sample daughter board, and digital signal processing FPGA board. The top layer is RF signal modulation front end.

The 162.5 MHz radio frequency signal of the signal generator's output is divided into three ways by power splitter. The first one is as reference input of AD9858 DDS function board, which reconstructs 30.72 MHz intermediate frequency. The second one is down converted into 130.78 MHz local oscillator signal by a mixer and a band pass filter. The third one is as reference signal of LLRF control system. So there are four independently down conversion circuit modules, one up conversion circuit module, and one level matching amplifier module link.

All digital signal processing and loop control algorithms of LLRF control system are completed in Stratix-III FPGA signal processing platform, which consist of a High-performance Stratix III EP3SL150F1152 FPGA, two data conversion high-speed mezzanine cards (HSMC) with 4 ways MAX sample speed 150MSPS 14 bits ADCs and 4 ways MAX conversion speed 250MSPS DACs, and a Marvell 88e1111 device used for 10/100/1000 base-T Ethernet connection. To acquire signal phase and amplitude of IF signals, the four output data of ADCs are synchronously IQ detected, CIC filtered, and CORDIC calculated in FPGA. Then phase stability loop and amplitude stability loop is implemented with PI control by digitally adjusting phase word of NCO, and digitally modulating amplitude of NCO. The tuner controller is supplied with three digital signals (pulse, direction and enable) for step motor, by real-time calculating the phase error between transmission signal and reflected signal picked up from director, and PI algorithms.

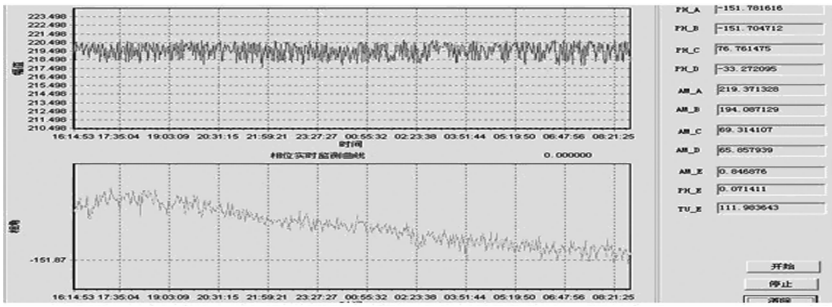

Fig. 2 LLRF twelve-hour amplitude stability and phase stability test result.

This LLRF control system is first generation based on completely digital IQ technology. The twelve-hour test results show(in Fig. 2) that the amplitude stability is 0.32%(peak to peak), ±0.18%(RMS), and the phase stability is ±0.35°(peak to peak), ±0.09°(RMS). In future, there will be much work to do, such as developing RF front end based on ICs, improving the reliability of LLRF, acquiring and debugging loop PI parameters in 4 K environment, optimizing algorithms, and so on. Although this LLRF is not so perfect, it performs well in room temperature in twelve-hour test.

6 - 10 RFQ Design of ADS Project at IMP

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China has launched its ADS (Accelerator Driven System) project since 2011 to deal with nuclear wastes and energy shortage problem. A high energy linear accelerator (LINAC) is necessary for the ADS. There are two front ends for the China's ADS LINAC, one of which will be built by IMP (Institute of Modern Physics). As one part of the front end, a four-vane RFQ has been designed in collaboration with LBNL (Lawrence Berkeley National Laboratory).

Table 1 Main parameters of ADS RFQ at IMP

Ion species	Proton
Frequency (MHz)	162.5
Input /Output energy (MeV)	0.035/2.1
Current (mA)	15
Input Emittance (nrms) (πmm • mrad)	0.3
Output trans. emittance (nrms) (πmm • mrad)	0.31
Output long. emittance (keV ns)	0.92
$\alpha_{in}/\alpha_{xout}$, α_{xout}	1.21/0.36, −0.3
Inter-vane voltage (kV)	65
K_p factor	1.2
Minimum aperture (mm)	3.2
Modulation	1～2.38
Synchronous phase (deg)	−90～−22.7
Cavity length (cm)	420.8
Transmission efficiency (%)	99.6

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